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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,823	ROCHE ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been considered. Claims 1-2, 4-5, 9, 11-12, 19, 21-22, 24-25, and 29 have been amended as per Applicant's request.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 10-12, 20-22, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Galvin et al. (herein Galvin), in view of *In re Japikse,* 181 F.2d 1019, 1023, 86 USPQ 70, 73 (CCPA 1950) (herein Japikse).

4. As per Claim 1, Galvin teaches: A microprocessor comprising:

a processing unit (Page 46, the "hardware");

a memory comprising a lower memory area and an extended memory area (Pages 48-49, also see Figure 2.7 which defines address spaces);

an address bus connecting said processing unit to said memory (inherent, also see page 30), and comprising a lower address bus for accessing said lower memory area and an extended address bus for accessing said extended memory area (See figure 2.7. A "bus" is just a collection of wires, and Examiner is interpreting the lower and extended address buses as the wires which allow access to the lower and

extended areas of the memory (as memory addresses get larger, more bits are required to address them, the other bits are not required, thus the bits required to address the highest locations in memory where protected memory may lie are considered the "extended" address bus), and Examiner finds support for this interpretation in Applicant's Figure 1, which only shows a single bus of 24 bits, thus the separation of the "lower" and "extended" buses would appear to be arbitrary and represent what Examiner laid forth above, as opposed to a distinct, physical separation, which would also imply distinct memories, which does not appear to be the case);

means for executing instructions of an instruction set executable by said processing unit, the instruction set comprising instructions for accessing said addressable memory space (Pages 48-49), a first instruction group comprising instructions for accessing said lower memory area (Page 46, user mode instructions), and a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing said extended memory area (Page 46, privileged instructions); and

means for preventing said extended address bus from accessing said extended memory area when executing an instruction in the first instruction group (Pages 48-49, access outside the specified memory area in user mode is prevented).

While Galvin teaches an extended and lower memory area, an address bus to connect the memory to the processor, Galvin discloses that the protected (monitor) memory area, which has the restricted access, is at the "lower" end of the memory, and in the claimed invention, Galvin's protected memory would have to be at the "upper" end

of memory to fulfill the claims, with the assumption that "lower" and "extended" memory are not just labels, and representative of where in memory relative to each other they reside. However, this is just an implementation difference, and there is no reason one of ordinary skill in the art could not shift the locations around and have monitor code at the "top" of memory (or any other location). This is supported by Japikse, which indicates that a shifting of parts is not a patentable distinction. Given these teachings, one of ordinary skill in the art would have been motivated and capable of having monitor/protected code at the "top" of memory in Galvin's invention, thus making it the "extended" memory area.

5. As per Claim 2, Galvin teaches: A microprocessor according to claim 1, wherein each location in said addressable memory space is associated with a respective access address; the microprocessor further comprising means for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing an instruction in the first instruction group (Pages 48-49, an exception occurs when accessing memory out of bounds).

6. As per Claims 10, 20, and 30, with Claim 10 being exemplary, Galvin teaches a microprocessor according to claim 1, but fails to teach:

wherein said lower memory area is accessible over 16 bits and said extended memory area is accessible over 24 bits.

Galvin teaches an operating system method to address protected memory, and in Figure 2.7 on Page 48, shows several segments of memory, with the "extended" or protected mode in the lower section of the memory, where the "lower" section of memory as claimed by the Applicant is actually addressed as "higher" memory locations. However, this is just an implementation difference, and there is no reason one of ordinary skill in the art could not shift the locations around and have monitor code at the "top" of memory. As each block gets "higher" into the memory, more and more bits are required to address it, thus, to access job 4's area in memory, more bits are required than to access job 1's area. For example, Job 1 can be addressed over 19 bits, and Job 4 is addressed over 20 bits. In addition, changing bit size is not considered to be a patentable distinction. See *In re Rose,* 200 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955). Claims 20 and 30 teach similar limitations and are rejected for the same reason.

7. As per Claim 11, Galvin teaches: A microprocessor comprising:

a processing unit (Page 46, the "hardware");

a memory comprising a lower memory area and an extended memory area (Pages 48-49, also see Figure 2.7 which defines address spaces);

an address bus connecting said processing unit to said memory (inherent, also see Page 30), and comprising a lower address bus for accessing said lower memory area and an extended address bus for accessing said extended memory area (See figure 2.7. A "bus" is just a collection of wires, and Examiner is interpreting the lower

and extended address buses as the wires which allow access to the lower and extended areas of the memory (as memory addresses get larger, more bits are required to address them, the other bits are not required, thus the bits required to address the highest locations in memory where protected memory may lie are considered the "extended" address bus), and Examiner finds support for this interpretation in Applicant's Figure 1, which only shows a single bus of 24 bits, thus the separation of the "lower" and "extended" buses would appear to be arbitrary and represent what Examiner laid forth above, as opposed to a distinct, physical separation, which would also imply distinct memories, which does not appear to be the case) and

a set of instructions executable by said processing unit, the set of instructions comprising

a first instruction group comprising instructions for accessing said lower memory area (Page 46, user mode instructions),

a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing said extended memory area (Page 46, privileged instructions); and

means for preventing said extended address bus from accessing said extended memory area when executing an instruction in the first instruction group (Pages 48-49, access outside the specified memory area in user mode is prevented).

While Galvin teaches an extended and lower memory area, an address bus to connect the memory to the processor, Galvin discloses that the protected (monitor) memory area, which has the restricted access, is at the "lower" end of the memory, and

in the claimed invention, Galvin's protected memory would have to be at the "upper" end of memory to fulfill the claims, with the assumption that "lower" and "extended" memory are not just labels, and representative of where in memory relative to each other they reside. However, this is just an implementation difference, and there is no reason one of ordinary skill in the art could not shift the locations around and have monitor code at the "top" of memory (or any other location). This is supported by Japikse, which indicates that a shifting of parts is not a patentable distinction. Given these teachings, one of ordinary skill in the art would have been motivated and capable of having monitor/protected code at the "top" of memory in Galvin's invention, thus making it the "extended" memory area.

8. As per Claim 12, Galvin teaches: A microprocessor according to claim 11, wherein each location in said addressable memory space is associated with a respective access address; and the microprocessor further comprising means for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing an instruction in the first instruction group (Pages 48-49, an exception occurs when accessing memory out of bounds).

9. As per Claim 21, Galvin teaches: A method for accessing a memory used by a microprocessor, the memory comprising a lower memory area and an extended memory area (Pages 48-49, also see Figure 2.7 which defines address spaces), the microprocessor comprising a processing unit (Page 46, the "hardware"), an address bus

for connecting connected the processing unit to the memory (inherent, also see page 30), and comprising a lower address bus for accessing the lower memory area and an extended address bus for accessing the extended memory area, the method comprising (See figure 2.7. A "bus" is just a collection of wires, and Examiner is interpreting the lower and extended address buses as the wires which allow access to the lower and extended areas of the memory (as memory addresses get larger, more bits are required to address them, the other bits are not required, thus the bits required to address the highest locations in memory where protected memory may lie are considered the "extended" address bus), and Examiner finds support for this interpretation in Applicant's Figure 1, which only shows a single bus of 24 bits, thus the separation of the "lower" and "extended" buses would appear to be arbitrary and represent what Examiner laid forth above, as opposed to a distinct, physical separation, which would also imply distinct memories, which does not appear to be the case):

executing an instruction for accessing the lower memory area, the instruction belonging to an instruction set comprising a first instruction group comprising instructions for accessing the lower memory area (Page 46, user mode instructions), and a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing the extended memory area (Page 46, privileged instructions);

preventing access to the extended memory area when executing an instruction in the first instruction group (Pages 48-49, access outside the specified memory area in user mode is prevented).

While Galvin teaches an extended and lower memory area, an address bus to connect the memory to the processor, Galvin discloses that the protected (monitor) memory area, which has the restricted access, is at the "lower" end of the memory, and in the claimed invention, Galvin's protected memory would have to be at the "upper" end of memory to fulfill the claims, with the assumption that "lower" and "extended" memory are not just labels, and representative of where in memory relative to each other they reside. However, this is just an implementation difference, and there is no reason one of ordinary skill in the art could not shift the locations around and have monitor code at the "top" of memory (or any other location). This is supported by Japikse, which indicates that a shifting of parts is not a patentable distinction. Given these teachings, one of ordinary skill in the art would have been motivated and capable of having monitor/protected code at the "top" of memory in Galvin's invention, thus making it the "extended" memory area.

10. As per Claim 22, Galvin teaches: A method according to claim 21, wherein each location in the addressable memory space is associated with a respective access address; the method further comprising forcing an access address of a location to be accessed to point to a location in the lower memory area when executing an instruction in the first instruction group (Pages 48-49, an exception occurs when accessing memory out of bounds).

11. Claims 3-4, 13-14, and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Galvin and Japikse, in view of Suleman.

12. As per Claim 3, Galvin teaches: A microprocessor according to claim 1, further comprising at least one internal register (Examiner is taking official notice that a register file, and thus internal registers, are in almost every processing machine that executes instructions and operates a memory, and would have been in the system intended for Galvin's invention), but fails to teach:

wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said addressable memory space; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

Galvin teaches a system to address a memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Galvin's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

13. As per Claim 4, Galvin teaches: A microprocessor according to claim 1, wherein each location in said addressable memory space is associated with a respective access address (Page 48); and

The microprocessor further comprising means for maintaining an address of a jump destination location so that it points to a location in said lower memory area (Pages 48-49, a user mode instruction can not have a destination that legally points outside of its range), but fails to teach:

for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area.

Galvin teaches a system to address a memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Galvin's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

14. As per Claim 13, Galvin teaches: A microprocessor according to claim 11, further comprising at least one internal register (Examiner is taking official notice that a register file, and thus internal registers, are in almost every processing machine that executes

instructions and operates a memory, and would have been in the system intended for Galvin's invention), but fails to teach:

wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said addressable memory space; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

Galvin teaches a system to address a memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Galvin's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

15. As per Claim 14, Galvin teaches: A microprocessor according to claim 11, wherein each location in said addressable memory space is associated with a respective access address (Page 48); and

said instruction set further comprises instructions for maintaining an address of a jump destination location so that it points to a location in said lower memory area

(Pages 48-49, a user mode instruction can not have a destination that legally points outside of its range), but fails to teach:

executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area.

Galvin teaches a system to address a memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Galvin's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

16. As per Claim 23, Galvin teaches: A method according to claim 21, wherein the microprocessor further comprises at least one internal register (Examiner is taking official notice that a register file, and thus internal registers, are in almost every processing machine that executes instructions and operates a memory, and would have been in the system intended for Galvin's invention), but fails to teach:

wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in the addressable memory space; and

data transfer instructions between the arbitrary memory location and the at least one internal register.

Galvin teaches a system to address a memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Galvin's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

17. As per Claim 24, Galvin teaches: A method according to claim 21, wherein each location in the addressable memory space is associated with a respective access address (Page 48);

the method further comprising maintaining an address of a jump destination location so that it points to a location in the lower memory area (Pages 48-49, a user mode instruction can not have a destination that legally points outside of its range), but fails to teach:

for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in the lower memory area.

Galvin teaches a system to address a memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in

the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Galvin's invention was to be implemented in an 8086 machine in order to take advantage of the operating system, then they would have Jump, Call, and Move instructions available to them.

18. Claims 5-9, 15-19, and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Galvin and Japikse, in view of Official Notice.

19. As per Claim 5, Galvin teaches: A microprocessor according to claim 1, the microprocessor further comprising means for forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in said lower memory area and points to this area (Pages 48-49, the program would be terminated if the address was illegal, "forcing" it to point to correct areas in order to execute), but fails to teach:

wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area.

While Galvin teaches a high-level view of a computer system utilizing an operating system with instructions to access memory, indirect addressing is not explicitly taught for the systems on which the teachings operate, as it is beyond the scope of the textbook. However, the concept of indirect addressing is well known in the

art, and implemented in many instruction sets, and Examiner is taking Official Notice that one of ordinary skill in the art would have been able to make use of indirect addressing instructions to run on a system such as Galvin's to address memory.

20. As per Claim 6, Galvin teaches: A microprocessor according to claim 1, wherein the second instruction group comprises instructions for accessing said extended memory area (Page 46, privileged instructions), but fails to teach:

in an indirect addressing mode (see Claim 5 rejection).

21. As per Claim 7, Galvin teaches: A microprocessor according to claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area (Pages 48-49 states that in protected mode (able to address extended memory area), there are no memory limitations, thus the pointers could be located anywhere, including the lower area).

22. As per Claim 8, Galvin teaches: A microprocessor according to claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area (Pages 48-49 states that in protected mode (able to address extended memory area), there are no memory limitations, thus the pointers could be located

anywhere, including the extended area).

23. As per Claim 9, Galvin teaches: A microprocessor according to claim 1, further comprising a program pointer register having a size corresponding to a size of said address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in said addressable memory space (inherent for any machine to have a register to enable access to the memory of the required size).

24. As per Claim 15, Galvin teaches: A microprocessor according to claim 11, wherein said instruction set further comprises instructions for forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in said lower memory area and points to this area (Pages 48-49, the program would be terminated if the address was illegal, "forcing" it to point to correct areas in order to execute), but fails to teach:

wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area.

While Galvin teaches a high-level view of a computer system utilizing an operating system with instructions to access memory, indirect addressing is not explicitly taught for the systems on which the teachings operate, as it is beyond the scope of the textbook. However, the concept of indirect addressing is well known in the art, and implemented in many instruction sets, and Examiner is taking Official Notice that one of ordinary skill in the art would have been able to make use of indirect

addressing instructions to run on a system such as Galvin's to address memory.

25. As per Claim 16, Galvin teaches: A microprocessor according to claim 11, wherein the second instruction group comprises instructions for accessing said extended memory area (Page 46, privileged instructions) in an indirect addressing mode (see Claim 15 rejection).

26. As per Claim 17, Galvin teaches: A microprocessor according to claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area (Pages 48-49 states that in protected mode (able to address extended memory area), there are no memory limitations, thus the pointers could be located anywhere, including the lower area).

27. As per Claim 18, Galvin teaches: A microprocessor according to claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area (Pages 48-49 states that in protected mode (able to address extended memory area), there are no memory limitations, thus the pointers could be located anywhere, including the extended area).

28. As per Claim 19, Galvin teaches: A microprocessor according to claim 11, further comprising a program pointer register having a size corresponding to a size of said address bus (This would be required, for a high-level view of this, see page 30, Figure 2.1) for enabling access to a program instruction to be executed that is located at an arbitrary location in said memory (inherent for any machine to have a register to enable access to the memory of the required size).

29. As per Claim 25, Galvin teaches: A method according to claim 21, the method further comprising forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in the lower memory area and points to this area (Pages 48-49, the program would be terminated if the address was illegal, "forcing" it to point to correct areas in order to execute), but fails to teach:

wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in the lower memory area.

While Galvin teaches a high-level view of a computer system utilizing an operating system with instructions to access memory, indirect addressing is not explicitly taught for the systems on which the teachings operate, as it is beyond the scope of the textbook. However, the concept of indirect addressing is well known in the art, and implemented in many instruction sets, and Examiner is taking Official Notice that one of ordinary skill in the art would have been able to make use of indirect addressing instructions to run on a system such as Galvin's to address memory.

30. As per Claim 26, Galvin teaches: A method according to claim 21, wherein the second instruction group comprises instructions for accessing the extended memory area (Page 46, privileged instructions) in an indirect addressing mode (see Claim 25 rejection).

31. As per Claim 27, Galvin teaches: A method according to claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located in the lower memory area (Pages 48-49 states that in protected mode (able to address extended memory area), there are no memory limitations, thus the pointers could be located anywhere, including the lower area).

32. As per Claim 28, Galvin teaches: A method according to claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located within the extended memory area (Pages 48-49 states that in protected mode (able to address extended memory area), there are no memory limitations, thus the pointers could be located anywhere, including the extended area).

As per Claim 29, Galvin teaches: A method according to claim 21, wherein the microprocessor further comprises a program pointer register having a size corresponding to a size of the address bus (This would be required, for a high-level view

of this, see page 30, Figure 2.1) for enabling access to a program instruction to be executed that is located at an arbitrary location in the memory (inherent for any machine to have a register to enable access to the memory of the required size).

Response to Arguments

33. Applicant's have argued that Galvin fails to teach an extended address bus for accessing an extended memory area, and cannot restrict legal memory to a lower area due to the interrupt (monitor) code being stored in the "low" sections of memory as described by Galvin. However, as previously stated in the rejections for Claims 10/20/30 in the previous action, and in the independents in the current action, the exact location of the monitor code is a design choice and is not constrained to the lowest addressable locations of memory, and in Examiners current interpretation of Galvin with that in mind is that the monitor code is in the top-most sections of memory, such that legal memory can be bounded, and in this interpretation, "extended" memory, being represented by the "top" of memory, does contain the restricted portions of the memory.

Applicant has further argued that Galvin does not teach two groups of instructions, with one group accessing only the lower memory, and the other group containing all the instructions for accessing the extended memory area. However, Examiner asserts that Galvin does teach these two distinct groups in user-mode and privileged instructions, as user-mode instructions can only access legal memory, and privileged instructions have the option of accessing protected memory (thus contains all

of the instructions for accessing the extended memory area), which makes the two different types of instructions different groups as defined in the claim.

Applicant's remaining arguments have essentially asserted that Galvin does not teach extending the memory space of a memory, nor to maintain compatibility of old programs, however, while this may be the intent of the invention, these features are not represented in the claims, and appear to be an intended use of the invention even if they were. Furthermore, despite Galvin requiring two additional registers to perform this protection of memory, there is no language in the claims that indicates that registers cannot be used to perform this method.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:45-6:15.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema
Examiner
Art Unit 2183

RF

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100